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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,495	08/31/2006	Tae-Pok Rhee	2017-111	6355

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EXAMINER	
HSIEH, HSIN YI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,495	RHEE, TAE-POK	
	Examiner	Art Unit	
	Hsin-Yi (Steven) Hsieh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060831*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 08/31/2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of "an active area", "a step of driving-in the low concentration impurity layer" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: claim 5 recites "the gate electrode pattern maintains a width wider than the device separating film. There is no disclosure in the specification of the detail of this limitation.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 recites "the gate electrode pattern maintains a width wider than the device separating film. There is no disclosure in the specification of the detail of this limitation.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 1 recites the limitation "which area" in the fourth line of the claim. There is insufficient antecedent basis for this limitation in the claim.

11. Claims 2-6 are rejected because they depend on the rejected claim 1.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. **Claims 1-2 and 4-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Min (US 6,476,444 B1) and in view of Nakajima et al. (US 4,931,409 A) as can be understood since claims 1-6 have been rejected under 35 U.S.C. 112.

15. Regarding **claims 1 and 2**, Min teaches a semiconductor device of high breakdown voltage (semiconductor device; Abstract) comprising: a gate electrode pattern (gate electrode 34; Fig. 2I, col. 3 line 27) embedded in an active area (the area between the areas of 27s; Fig. 2I, col. 3 line 30) of a semiconductor substrate (21; Fig. 2A-2I, col. 3 line 28), which area is defined by a device separating film (device isolation layer 27; col. 3 lines 27-29); a gate insulating layer pattern (first gate trench sidewall 31, an oxide film, and gate oxide film 33; Fig. 2I, col. 3 lines 19 and 29) surrounding the gate electrode pattern (34; see Fig. 2I); high concentration impurity layers (heavily doped impurity region 37; Fig. 2I, col. 4 lines 39-40) located on both sides of the gate electrode pattern (34) to contact the gate insulating layer pattern (31 and 33) and formed in an upper layer (37) of the active area (the area between 27s) of the semiconductor substrate (21; see Fig. 2I for the structure relationships) by an ion implantation (process limitation in the product claim which has no patentable weight); and low concentration impurity layers (lightly

doped impurity region 36; Fig. 2I, col. 4 lines 38) located on both sides of the gate electrode pattern (34) to contact the gate insulating layer pattern (31 and 33) and formed under the high concentration impurity layers (37; see Fig. 2I for the structure relationships) by an ion implantation (process limitation in the product claim which has no patentable weight).

Min does not teach, regarding to **claim 1**, a device separating film having an inversion preventing layer, and regarding to **claim 2**, the high concentration impurity layers are separately formed so as not to electrically contact the inversion preventing layer of the device separating film.

In the same field of endeavor of trench isolation, Nakajima et al. teach, regarding to **claim 1**, a device separating film (SiO2 film 17; Fig. 2D, col. 5 line 64) having an inversion preventing layer (p+-type layer 18; col. 6 lines- 11), and regarding to **claim 2**, the high concentration impurity layers (N+-type buried layer 12; Fig. 2D, col. 5 line 46) are separately formed ("separately formed" is a process limitation in the product claim and has no patentable weight) so as not to electrically contact the inversion preventing layer (18) of the device separating film (17; see Fig. 2D).

Nakajima et al. also teach the inversion preventing layer is used to prevent the degradation in leakage and breakdown voltage between elements (col. 1 lines 19-24).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Min and Nakajima et al. and use a device separating film having an inversion preventing layer as taught by Nakajima et al., because the degradation in leakage and breakdown voltage between elements can be prevented as taught by Nakajima et al.

16. Regarding **claim 4**, Min also teaches the device according to claim 1, wherein the gate electrode pattern (34) is embedded in a depth shallower than the device separating film (27; see Fig. 2I).

17. Regarding **claim 5**, Min does not teach the gate electrode pattern (34) maintains a width wider than the device separating film (27).

Parameters such as widths of the gate electrode pattern and the device separating film in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance. For example, the width of the gate electrode are determined by the desired driving current and leakage current, while the width of the device separating film is determined by the desired leakage. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the width of the gate electrode pattern wider than the width of the device separating film in order to fulfill the requirement of a specific driving current and leakage.

18. Regarding **claim 6**, Min also teaches the device according to claim 1, further comprising a threshold voltage control layer provided in a bottom of the gate insulating layer pattern (33) for controlling a threshold voltage of a channel formed by the gate insulating layer pattern (33) (Min discloses a step of ion implantation for adjusting the device threshold voltage in col. 4 lines 30-32 and Fig. 2H. From Fig. 2H, the channel, which is at the bottom of the gate insulating layer, is exposed to the implantation and receives the implant, which is the threshold voltage control layer, though it is not shown in Fig. 2H).

19. Regarding **claim 7**, Min also teaches a method of manufacturing a semiconductor device of high breakdown voltage comprising (semiconductor device; Abstract) steps of: forming a

trench (first gate trench 30; Fig. 2G to 2I) in an active area (the area between the areas of 27s; Fig. 2I, col. 3 line 30) of a semiconductor substrate (21; Fig. 2A-2I, col. 3 line 28); forming a gate insulating layer pattern (first gate trench sidewall 31, an oxide film, and gate oxide film 33; Fig. 2I, col. 3 lines 19 and 29) on a surface of the trench (30); forming a gate electrode pattern (gate electrode 34; Fig. 2I, col. 3 line 27) in the trench (30) to contact the gate insulating layer pattern (31 and 33; see Fig. 2I); forming low concentration impurity layers (lightly doped impurity region 36; Fig. 2I, col. 4 lines 38) in the active area (the area between the areas of 27s; Fig. 2I, col. 3 line 30) of the semiconductor substrate (21) to contact the gate insulating layer pattern (33) and to be located on both sides of the gate electrode pattern (34) by an ion implantation (injecting impurities; col. 4 line 40); and forming high concentration impurity layers (heavily doped impurity region 37; Fig. 2I, col. 4 lines 39-40) on the low concentration impurity layers (36) to contact the gate insulating layer pattern (33) and to be located on both sides of the gate electrode pattern (34; see Fig. 2I) by an ion implantation (injecting impurities; col. 4 line 40).

20. Regarding **claim 8**, Min also teaches a step of forming a threshold voltage control layer in a bottom of the gate insulating layer pattern (33) for controlling a threshold voltage of a channel formed by the gate insulating layer pattern (33) (Min discloses a step of ion implantation for adjusting the device threshold voltage in col. 4 lines 30-32 and Fig. 2H. From Fig. 2H, the channel, which is at the bottom of the gate insulating layer, is exposed to the implantation and receives the implant, which is the threshold voltage control layer, though it is not shown in Fig. 2H).

21. Regarding **claim 9**, Min does not teach the gate insulating layer pattern is formed to have a thickness of 180Å~2500Å.

Parameters such as the thickness of the of the gate insulating layer pattern in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thickness of the of the gate insulating layer pattern within the range as claimed in order to form a high quality film.

22. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Min and Nakajima et al. as applied to claim 1 above, and further in view of Lee (US 6,638,825 B2) as can be understood since claims 1-6 have been rejected under 35 U.S.C. 112.

23. Regarding **claim 3**, Min and Nakajima et al. do not teach junctions of the low concentration impurity layers are formed at a depth equal to or deeper than the depth of the embedded gate electrode pattern by the ion-implantation.

In the same field of endeavor of MOS transistors, Lee teaches junctions (junctions between semiconductor substrate 31 and drift ion injection region 32; Fig. 3P, col. 3 lines 45-46 and 53) of the low concentration impurity layers (a drift ion injection region 32; Fig. 3P, col. 3 lines 45-46) are formed at a depth equal to or deeper than the depth of the embedded gate electrode pattern (gate electrode 42a; Fig. 3P, col. 5 line 26) by the ion-implantation (ion implantation is a process limitation in the product claim and has no patentable weight).

Lee also teaches the structure improves voltage-resistant characteristics and reduces the size of a device in order to improve packing density (col. 2 lines 34-39).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Min, Nakajima et al. and Lee by using the structure of junctions of the low concentration impurity layers formed at a depth equal to or deeper than the depth of the embedded gate electrode pattern as taught by Lee, because the packing density can be improved as taught by Lee.

24. **Claim 10-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Min and Nakajima et al. as applied to claim 7 above, and further in view of Malhi et al. (US 5,304,827 A).

25. Min and Nakajima et al. do not teach, regarding to **claim 10**, a step of driving-in the low concentration impurity layers at high temperatures, regarding to **claim 11**, the step of driving-in the low concentration impurity layers is performed at 1000°C~1250°C, and regarding to **claim 12**, the step of driving-in the low concentration impurity layers is performed for 30 min.~600 min.

In the same field of endeavor of MOS transistors, Malhi et al. teach, regarding to **claim 10**, a step of driving-in the low concentration impurity layers (source regions 34 and 36; Fig. 3 to Fig. 6, col. 3 lines 40-45) at high temperatures (1100°C; col. 3 lines 40-45), regarding to **claim 11**, the step of driving-in the low concentration impurity layers (34 and 36) is performed at 1000°C~1250°C (1100°C; col. 3 lines 40-45), and regarding to **claim 12**, the step of driving-in the low concentration impurity layers (34 and 36) is performed for 30 min.~600 min. (500 minutes; col. 3 lines 40-45).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Min, Nakajima et al. and Malhi et al. by using the drive-in

process as taught by Malhi et al., because this step is a well known option in the fabrication of low concentration impurity region of the fabrication of transistors as shown by Malhi et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HH
12/17/2007

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